Channel Characterization for Chip-scale Wireless Communications within Computing Packages

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Abstract—**Wireless Network-on-Chip (WNoC) appears as a promising alternative to conventional interconnect fabrics for chip-scale communications. WNoC takes advantage of an overlaid network composed by a set of millimeter-wave antennas to reduce latency and increase throughput in the communication between cores. Similarly, wireless inter-chip communication has been also proposed to improve the information transfer between processors, memory, and accelerators in multi-chip settings. However, the wireless channel remains largely unknown in both scenarios, especially in the presence of realistic chip packages. This work addresses the issue by accurately modeling flip-chip packages and investigating the propagation both its interior and its surroundings. Through parametric studies, package configurations that minimize path loss are obtained and the trade-offs observed when applying such optimizations are discussed. Single-chip and multi-chip architectures are compared in terms of the path loss exponent, confirming that the amount of bulk silicon found in the pathway between transmitter and receiver is the main determinant of losses.**

I. Introduction

Recent years have witnessed a rising interest towards heterogeneous multi-chip architectures and the so-called 2.5D integration. The reasons are various, but mostly have their origin in the diminishing returns of transistor scaling and the cost of manufacturing large chips. In this context, heterogeneous multi-chip architectures allow to increase *performance* of multicore processors beyond the limits of a large monolithic chip [1]; reduce their manufacturing *cost* by disintegrating a large monolithic chip into a network of smaller ones, but with much better yield [2]; and provide *versatility* or even *modularity* in response to the increasing appeal of co-integrating diverse components such as CPUs, GPUs, memories, or accelerators within a single package [3].

The new integration trends have strong consequences on the design of the communications backbone within the package. On the one hand, with the recent introduction of silicon interposers in 2.5D processes, there has been a reduction of the performance and cost difference between on-chip and off-chip communication [4]. Also, interposers may be capable of hosting *off-chip routers* in the future [2]. On the other

hand, increased system heterogeneity implies higher versatility requirements as the actual communication needs will depend on the actual constituents of the architecture.

It is expected that within-package networks will exploit the interposer advantages and rely on a tighter integration of the on-chip and off-chip sub-systems [2]. However, as off-chip transfers keep being expensive, it remains unknown whether such approach alone will suffice to meet the requirements of this scenario. As a result, emerging interconnect technologies are being explored as well [5], [6]. Among them, wireless chip-scale communications show great promise due to its inherent lack of path infrastructure. This allows to overcome pin limitations and contribute to versatility by providing low-latency broadcast capabilities across the package [7].

Research in highly-integrated wireless communications has exploded in the last decade [8]–[17]. The heterogeneous integration tendency has also impacted on this field, leading to several works of that explicitly consider wireless communications across chips for CPU-GPU coordination [18], integrated memory access [19], [20], or in a more generic intra-/inter-chip framework [21].

A missing piece in the wireless chip-scale puzzle is, however, the characterization of the wireless channel. The theory is well laid out [22] and a wide variety of works exist at on-chip [23]–[25], off-chip [26]–[28] and PCB board levels [29]–[31]. However, as detailed in Section V, very few studies include the chip package in their simulations or measurements and, those that do it, are limited to low frequencies or lack proper justifications on the antenna type and placement [32]–[34]. Note that, without proper understanding of the wireless channel within package, the path loss and dispersion assumptions may be overly optimistic. This affects the transceiver design and leads to inaccurate performance and efficiency reports. As most architectural studies rely in such figures, the impact of the wireless chip-scale paradigm cannot be really assessed.

This paper aims to address this issue by providing a characterization of wireless channels compatible with heterogeneous 2.5D packaging. We rigorously model the package in a variety of single-chip and multi-chip configurations and discuss the antenna placement. By means of full-EM simulation, we extract the field distribution and coupling between antennas and then derive path loss models. Through parametric studies, we obtain optimal package dimensions for path loss minimization
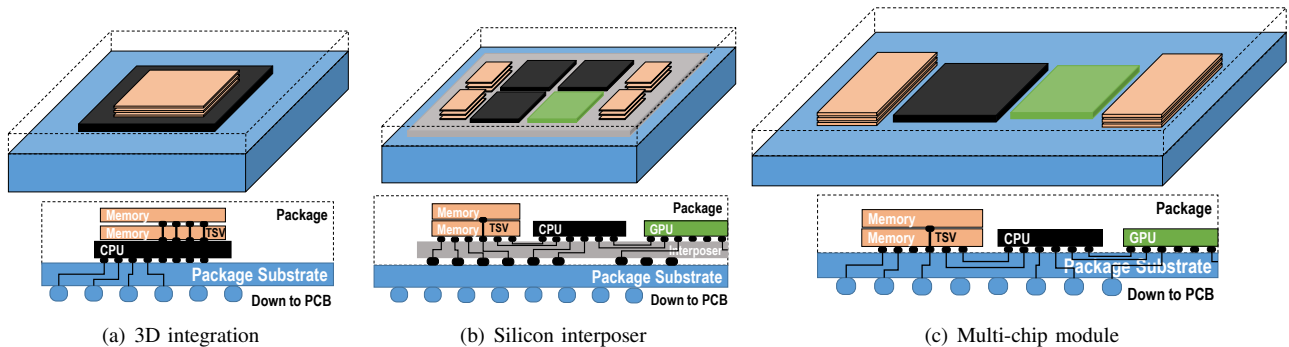
Fig. 1. Different heterogeneous integration techniques in examples with CPUs, GPUs, and memory. In a wireless approach, selected components would be equipped with one or several integrated antennas for wireless communication within the package.

and also analyze the impact of the die-package transitions in multi-chip configurations. Although the methodology is applicable to any antenna type and frequency range, we particularize it for the promising case of Through-Silicon Vias (TSVs) used as monopoles in the range of 50–150 GHz.

The remainder of the paper is as follows. Section II presents the system model, including details of the chip package and main assumptions. Section III describes the simulation methodology and subsequent channel modeling, whereas Section IV presents the main results. Finally, Section V analyzes related works and Section VI concludes the paper.

II. SYSTEM MODEL

This work considers a variety of multi-chip configurations for the channel characterization, summarized in Figure 1. All cases assume flip-chip integration. Although heat dissipation schemes are generally applied on a per-chip basis, here we propose the addition of a single heat spreader common to all chips and then the heat sink on top. Next, we provide more details on the structure of the package, dimensions, and materials.

A. Multi-chip Integration

The (heterogeneous) integration of multiple chips currently takes place either vertically or horizontally. The former, represented in Figure 1(a), consists on the stacking of several chips that have been previously thinned down below 100 μm [35]. Once stacked, the chips are interconnected through a forest of vertical TSVs with very fine pitch. This provides a huge bandwidth density and efficiency due to the very short link lengths. On the downside, 3D integration suffers from evident heat dissipation issues and the available area of integration basically depends on the dimensions of the chip at the base, i.e. around $20{\times}20$ mm^2.

Contrary to 3D stacking, heterogeneous 2.5D integration takes a co-planar approach and interconnects chips either through a common platform [4]. Depending on the level of integration, this common platform may be silicon interposer (Fig. 1(b)) or the package substrate in a more classical Multi-Chip Module (MCM) approach (Fig. 1(c)). Such an arrangement alleviates the heat dissipation issue of 3D stacking

and also increases the available area, as the limit is now set by the interposer ($24{\times}36$ mm^2 in [2], $40{\times}40$ mm^2 in [4]) or the substrate ($77{\times}77$ mm^2 in [1]). It also reduces the cost of the interconnects, as the pitch of TSVs is significantly coarsened. The main downturn of the approach is the reduction of bandwidth density and efficiency due to pin limitations and the need for longer links.

As for heat dissipation, it is worth noting that heat dissipation schemes are generally applied to each chip individually and then covered by a common lid. Instead, in his work we propose the addition of a single heat spreader common to all chips of a multi-chip configuration, and then a single heat sink on top. This would enhance heat dissipation further and favor inter-chip propagation through a common layer, reducing losses due to reflections at the chip-package interfaces. Molding compounds are sometimes used to fill the gaps between chips and below the heat spreader [36]. However, due to its poor thermal behavior, we advocate to the direct interfacing of the chip with the heat spreader. The lateral space between chips is assumed to be filled with air or vacuum.

This paper explicitly considers wireless communication in 2.5D environments. To this end, we model the interposer and MCM cases and comparing them with single-chip architectures. Therefore, the 3D stacking case is also indirectly represented: a single-chip architecture with thin silicon can be seen as a 3D stack as long as the antenna is placed on the top layer, just before the heat spreader.

B. Flip-chip Package

Although a recent work suggests a packageless architecture [37], dies have historically included a package to (i) act as a space transformer for I/O pins, provide mechanical support to the dies, and (iii) for ease of testability and repairability. Some packages include a molding compound around the chip to improves mechanical stability [36], but its typically poor thermal conductivity discourages its use in hot architectures. In most cases, even the packageless one [37], the die can be contacted directly by a Thermal Interface Material (TIM) with a metallic heat sink on top, avoiding the use of the molding compound.
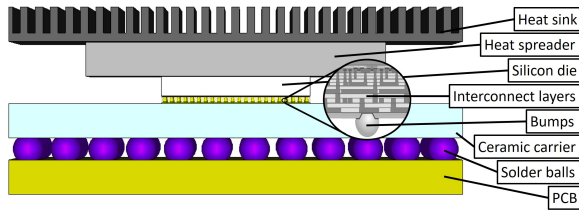
Fig. 2. Schematic of the layers of a flip-chip package

TABLE I
CHARACTERISTICS OF THE LAYERS IN A COMPUTING PACKAGE

	Thickness	Material	ε_r	$\tan(\delta)$
Heat sink	0.5 mm	Aluminum	-	-
Heat spreader	0.8 mm	Thermal cond.	8.6	$3\cdot10^{-4}$
Silicon die	0.2 mm	Bulk Silicon	11.9	0.2517
Interconnections	13 μm	Cu and **SiO$_2$**	3.9	0.03
Bumps	87.5 μm	Cu and Sn	-	-
Interposer	0.1 mm	Bulk Silicon	11.9	0.2517
Ceramic carrier	0.5 mm	Alumina	9.4	$4\cdot10^{-4}$

This work considers a flip-chip package with solder bumps. The packaging procedure is summarized here; we refer the reader to [38] and references therein for more details. During the manufacturing process, the solder bumps are deposited on the chip pads, which already carry a valid under bump metallization (UBM) like nickel/gold (Ni/Au). Then, the chip is flipped over and its solder bumps are aligned precisely to the pads of the package carrier external circuit. This is in contrast to wire bonding of chips on the package substrate or the interposer, in which the chip is mounted upright and wires are used to interconnect the chip pads to external circuitry [33]. Flip chip is generally preferred over wire bonding due to (i) its much lower inductance given by the shorter interconnect length [39], (ii) lower power–ground inductance due to direct routing of power, and (iii) higher power density given by the use of the whole chip surface.

An instance of the resulting complete package is shown in Figure 2. The layers are described from top to bottom as summarized in Table I. On top, the heat sink and heat spreader dissipate the heat out of the silicon chip, as they both have good thermal conductivity. Bulk silicon serves as the foundation of the transistors. This layer has low resistivity (10 Ω·cm), which is convenient for the operation of transistors, but not for electromagnetic propagation [40]. The interconnect layers, which occupy the bottom of the silicon die as shown in the inset of Fig. 2, are generally made of copper and surrounded by an insulator such as silicon dioxide (SiO$_2$) [41]. Depending on the case, we find a silicon interposer or a package substrate below the micro-bumps.

C. Package Optimization for EM Propagation

In our previous work, we discussed the impact of the different materials of a chip package on electromagnetic propagation. As pointed out above, the chip substrate and the heat spreader are the main determinants of the path loss and, by modifying their thicknesses, we can optimize propagation.
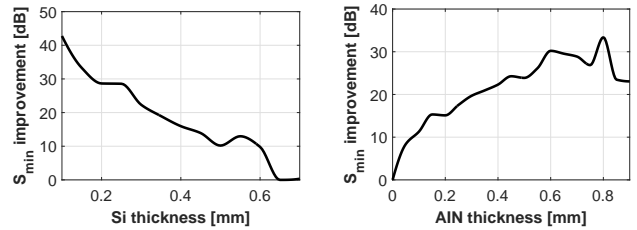
(a) Improvement over 0.7-mm Si   (b) Improvement over no AlN

Fig. 3. Adjusting the Silicon and heat spreader thickness result in huge improvements in the path loss.

The bulk silicon used in the chip substrate generally has low resistivity, which means a high loss tangent, and therefore we proposed to thin it to minimize propagation at this layer. To quantify the gains of this process, in [38] we studied the path loss for different silicon thickness values in a single-chip package. We took 100 μm as lower limit, frequently assumed in 3D stacking, although chip makers can reportedly reduce that further to tens of microns [42]. As we can see in Fig. 3(a), the path loss difference between the 0.1-mm and 0.7-mm cases is over 40 dB. Henceforth, we take 200 μm as the value by default.

The materials used as heat spreaders have good thermal properties and, coincidentally, low electrical losses [40]. To study their potential impact on electromagnetic propagation, in [38] we simulated a chip package with different heat spreader thicknesses –our choice was Aluminum Nitride (AlN). As observed in Fig. 3(b), thickening the heat spreader reduces losses up to 33 dB with respect to not having any heat spreader. Therefore, it is a parameter to consider in package engineering efforts. Henceforth, we consider a 800 μm AlN layer as the heat spreader by default.

D. Antenna Integration

The antenna placement within a flip-chip package is another important design consideration. Placing the radiating element as far from the lossy silicon as possible, as proposed in several works [23], [43], [44], is not realistic because the antenna would be short-circuited by the array of micro-bumps. Instead, printed dipoles [33] or patch antennas [45] may be implemented in the metal layers closest to the silicon. However, the proximity of the antennas to the *virtual ground plane* formed by the array of micro-bumps reduces their efficiency, whereas co-planarity between antennas further increases losses.

Finally, one could use TSVs as quarter-wave monopole antennas for several reasons: (i) the antenna would radiate laterally, directly towards the receiving antennas; (ii) advanced TSV and electroplating techniques [46] would allow fine-tuning the antenna to the desired frequency; and (iii) the array of micro-bumps would naturally act as a ground plane, allowing to see the quarter-wave monopole effectively as a dipole. Note that vertical on-chip monopoles have been proposed recently [47], but using non-standard fabrication and packaging.
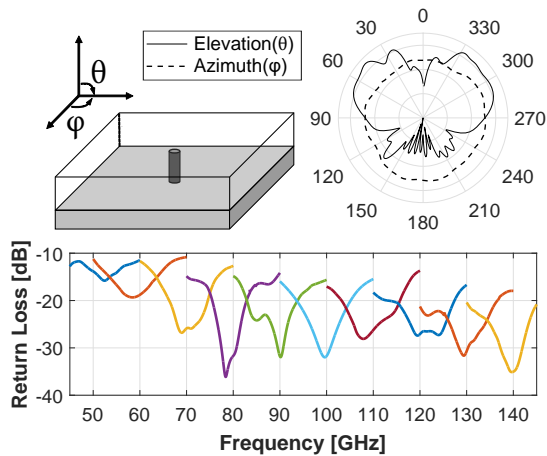
Fig. 4. Schematic representation of an on-chip monopole, expected radiation pattern, and return loss for instantiations optimized at 50–140 GHz.

Given the promising performance of monopoles in the chip-scale environment, we will consider them throughout this work. Figure 4 shows a sketch together with the expected radiation pattern within the package.

III. METHODOLOGY

The canonical structure of Fig. 2 is introduced in CST MWS [48] with the parameter values from Table I. We then modify the structure to model the different scenarios depicted in Fig. 1 and to perform package optimizations. To reduce the computational burden, we perform several approximations that do not affect the accuracy of the results. For instance, given their fine-grained pitched at mm-Wave frequencies, the micro-bump array placed between the chip and the package substrate/interposer is modeled as solid metallic element [38].

The monopole antenna is modeled as a thin and long cylindrical metallic structure, placed vertically passing through the silicon. Through optimization-driven simulations, the length of the monopole is adjusted to minimize the return loss at the central frequency of interest. By default, simulations are by default centered at 60 GHz with 20 GHz bandwidth. However, explorations at higher frequencies are also performed after the respective monopole length adjustments. Figure 4 shows the return loss of the different monopole instances.

Simulations consider a number of antennas evenly distributed across the chips. The outcomes are the field distribution, the antenna gain, and the coupling between antennas. Let $\overline{S_{ij}}$ be the average of the coupling between transmitter j and receiver i over the whole frequency band. The minimum of $\overline{S}$ is used as a benchmark to evaluate the worst case for several material thickness combinations. It can be expressed as:

$$S_{min} = \min_{i,j \neq i} \overline{S_{ij}}. \qquad (1)$$

With the S-parameters, the channel frequency response $H_{ij}(f)$ can be then evaluated for each antenna pair as

$$G_i G_j |H_{ij}(f)|^2 = \frac{|S_{ji}(f)|^2}{(1 - |S_{ii}(f)|^2) \cdot (1 - |S_{jj}(f)|^2)}, \qquad (2)$$

where G_i and G_j are the transmitter and receiver antenna gains, S_{ji} is the coupling between transmitter i and receiver j, whereas S_{ii} and S_{jj} are the reflection coefficients at both ends [49]. Once evaluated, a path loss analysis can be performed by fitting the attenuation over distance to

$$L_{dB} = 10n \cdot \log_{10}(d) + C, \qquad (3)$$

where d is the distance between antennas and n is the path loss exponent [23]. The path loss exponent is around 2 in free space, below 2 in guided or enclosed structures, and above 2 in lossy environments.

IV. SIMULATION RESULTS

In the following, we show the results of an extensive simulation study that explores the channel characteristics in single-chip and multi-chip settings. We perform package optimizations to minimize path loss and assess the impact of having a multiple chips on the optimal design point. Additionally, we explore the scaling with frequency.

A. On-chip wireless channel in single-chip package

We start by exploring the channel within a single-chip package. This models conventional processors, but also serves for 3D stacking if we assume that antennas are placed at the top chip –the one interfaced by the heat spreader. For this scenario, we consider a single square chip 22-mm long and wide, surrounded by conducting walls representing the package boundaries. The conducting walls are placed 5 mm away of the chip limits. The space between the chip and the walls is modeled as vacuum, although it could be filled with molding compound as discussed in Section II.

Package Optimization at 60 GHz. As indicated in Section II-C, it is preferable to keep the silicon thickness to a minimum and to increase that of the heat spreader. When introducing the antenna, results may oscillate and an antenna-package co-design may be required for optimization. Fig. 5(a) shows the results of such co-design, which keeping the monopole matched at 60 GHz at all times. It is found that the optimal silicon and AIN thicknesses are 0.10 mm and 0.85 mm, respectively, as they yield the highest mean of the worst case coupling. This shows that fine-grained optimization can provide extra 5–10 dB of path loss reduction.

Path loss at 60 GHz. To further highlight the importance of package optimization, we performed a path loss analysis at 60 GHz. We considered three different cases: default dimensions as specified in Table I, optimal dimensions as obtained in Fig. 5(a), and a quite suboptimal design point. Remind that the path loss decouples the antenna effects and leaves just losses due to propagation. The results, plotted in Figure 6, shows how optimization reduces not only the path loss overall, but also the path loss exponent. For the default case, the path loss exponent is 1.78, slightly lower than the free space path loss, thanks to having a confined environment. In the optimal case, we are able to cut the exponent down to 0.75, thereby showing a strong waveguiding effect in propagation. The suboptimal
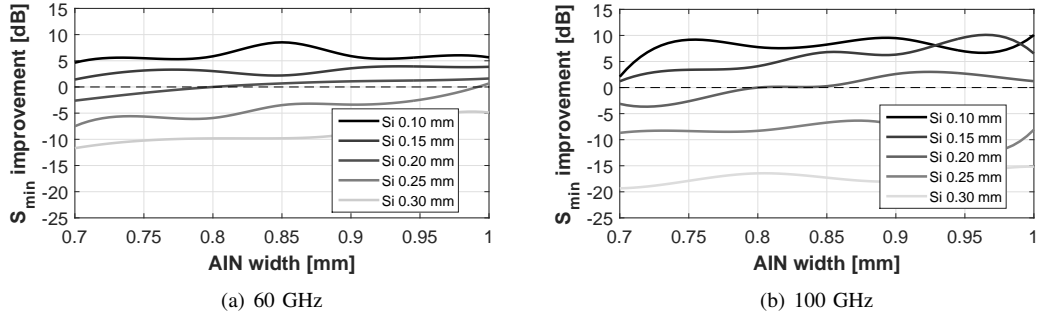
(a) 60 GHz

(b) 100 GHz

Fig. 5. Improvement of worst-case coupling S_{min} in the single-chip case at two frequency points. The baseline dimensions are specified in Table I.
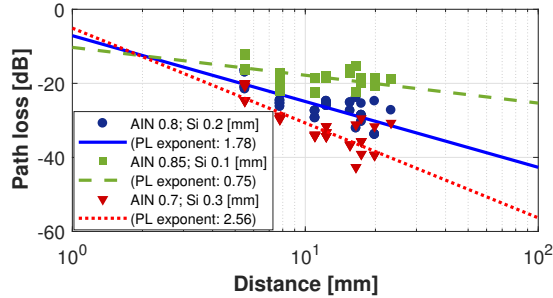

Fig. 6. Path loss as a function of distance, including linear regression fitting, for the single-chip case at 60 GHz.
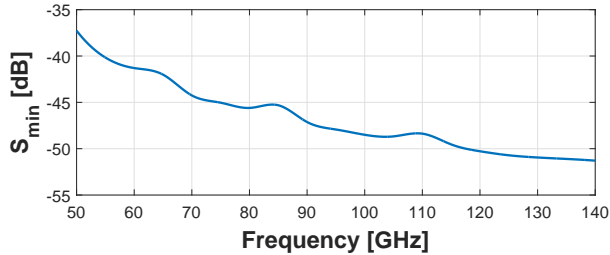

Fig. 7. Worst-case coupling S_{min} as a function of frequency in the single-chip case with the thicknesses specified in Table I.

case, with an exponent higher than 2, demonstrates that the losses introduced by silicon cannot be neglected.

Frequency sweep. Increasing the frequency of operation leads to smaller antennas and, potentially, smaller transceivers. Also, the absolute bandwidth is generally improved. Therefore, it is of great interest to study the scaling trends of the on-chip channel. Figure 7 shows how S_{min} scales over frequency. This sweep was performed with the default silicon and heat spreader widths, 0.2 mm and 0.8 mm, respectively. We can observe that in overall, the loss between links increases with frequency probably due to two reasons: the antennas have smaller apertures, and the propagation losses at the dielectrics are larger. Nevertheless, this effect is compensated in part by the enclosed nature of the on-chip scenario, mitigating the impacts of frequency scaling.

Impact of frequency on package optimization. Since our methodology performs a joint antenna-package optimization, it is reasonable to think that the optimal point will change with frequency. To illustrate this, we performed the exploration with the monopole tuned at 100 GHz. Figure 5(b) shows how the optimal point has slightly changed, but the tendency of higher losses with a thicker silicon is indeed, increased. This can be explained by the fact that losses on the silicon are frequency sensitive. Still, the improvement with respect to the default case is 10 dB and can be achieved even with 0.15mm of silicon.

B. On-chip wireless channel in multi-chip package

Let us now consider a single chip isolated in a package without lateral walls. This would *a priori* model the worst case for on-chip propagation in a multi-chip package, where lateral walls are far away and neighboring chips absorb most of the incoming energy. Indeed, the absence of reflecting elements nearby is expected to lead to a reduction of the energy that returns to the chip after leaving, therefore increasing the path loss. To evaluate this scenario, we consider a 22×22 mm^2 chip whose boundaries model a perfect matching layer (PML), giving the impression of an infinitely wide package without walls.

Impact of boundaries on loss between links. Without lateral walls, the loss of the worst-case link is increased up to 27 dB higher for the thicknesses of Table I (from -43 dB to -70 dB). This is due to the harsh reduction of the power received by the antenna at the opposite corner of the radiating one, as the majority of the power to this antenna was coming from the now non-existent reflections at the package walls. This results strongly suggests that, being either due to losses or security reasons (so that wireless signals cannot escape outside the package), having package walls is beneficial.

Impact of boundaries on package optimization. As we can see on Figures 8(a) and 8(b), the variation of S_{min} with respect to non-optimized case is large and more sensitive to the silicon thickness. Due to the absence of walls, package optimization plays an even more important role than with walls (Fig. 5). The improvement is larger than 20 dB in several cases. Note, also, that the exploration also unveiled very detrimental S_{min} dips at certain thickness combinations. See, for instance, the 0.1-mm silicon and 0.7-mm AIN case at 60 GHz in Figure 8(a).
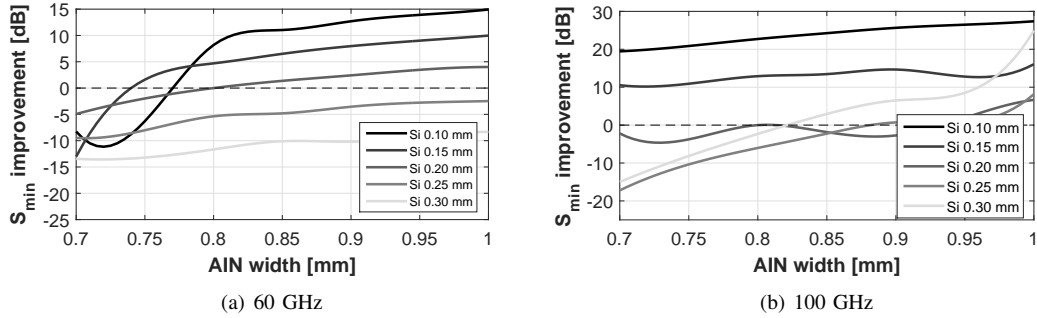
Fig. 8. Improvement of worst-case coupling S_{min} in the multi-chip case (without lateral walls) at two frequency points. The baseline dimensions are specified in Table I.

C. Off-chip wireless channel in multi-chip package

We finally consider a full multi-chip packages as represented in Figures 1(b) and 1(c). In the interposer case, we evaluate an array of 2×2 small chips, 10 mm in length each, placed inside a 33×33 mm² package with a separation of 5 mm between chips. The silicon interposer has 0.1 mm of thickness and 33 mm of length and width. In the MCM case, we simulate 2×2 chips of standard size, placed inside a bigger package whose length and width is 59 mm.

We place four antennas per chip, regardless of the chip size, in order to evaluate all the possible combinations, i.e., close or distant antennas in close or distant chips. All the multichip package simulations are performed with enclosing conducting walls and a common heat spreader for all chips.

Small chips vs single standard chip. The silicon interposer case allows us to evaluate the impact of processor disintegration [2] on the wireless channel characteristics. To this end, we compare the coupling between antennas in a single large chip, Fig. 9(a), and multiple small chips, Fig. 9(b). The plots do not illustrate large changes overall –a slightly better coupling is observed in the interposer case (only a few dBs in most antenna pairs, including S_{min}). There are two effects that seem to be canceling out: on the one hand, propagation occurring in the vacuum space between chips instead of in lossy silicon would lead to better coupling in the interposer case. On the other hand, reflections due to media changes (silicon–vacuum–silicon) are also higher in the interposer case, which may be leading to lower coupling in far away antennas. This may also explain the better coupling at nearby antennas (port 2 and 5).

Path loss: interposer vs MCM. The path loss exponent is calculated for the two multi-chip scenarios and compared with that of 3D stacking, previously shown in Fig. 6. In all cases, we considered the default thicknesses specified in Table I. The path loss exponent of the interposer scenario, plotted in Figure 10(a), is 1.55. This is slightly lower than the exponent of the single-chip case (1.78), thanks to the lack of silicon between chips. The path loss exponent increases up to 4.27 for MCM case, plotted in Fig. 10(b), due to the crescent losses due to propagation through lossy silicon as the distance between antennas increases. This confirms that the amount of silicon that waves need to traverse is the main determinant of losses.

V. RELATED WORK

Channels within a Chip Package: the existence of a wireless channel in flip-chip packages was suggested in [32] and then experimentally validated at 15 GHz in [33]. Recently, the work by Narde *et al.* analyzes the S-parameters for one and two chips within the same package assuming planar zig-zag antennas at 60 GHz [34]. Although becoming part of the radiative structure by capacitive coupling, the effect of bumps on the antenna response is not discussed. They also assume high-resistivity silicon, which may be unlikely in processor dies. Our previous works, instead, discuss different 60-GHz antenna types and perform field distribution and path loss analysis within a single-chip package with bulk silicon [38], [50]. The present work extends the frequency range up to 150 GHz and considers multiple single-chip and multi-chip configurations, both MCM and interposer-based.

Channels within a Metallic Casing: Matolak *et al.* suggested that the wireless chip-scale communications would act as a micro-reverberation chamber with metallic walls [22], although they did not discuss the package. Others have explored a similar scenario over a large PCB board, including DRAM modules and other components within a computer case up to 300 GHz [26], [29]–[31]. In [51], the authors explored waveguide-like millimeter-wave channels within a reconfigurable metamaterial that integrates multiple chips on a PCB. Finally, the 60-GHz channel has been also studied in larger enclosed environments such as printers [52] or data center cabinets [53], which also act as reverberation chambers. Although these structures may capture the enclosed nature of a chip package, they have substantially different dimensions, materials, and antenna placement restrictions.

Chip-scale Channels without Package: studies of the on-chip and off-chip wireless channels have been often conducted without considering any particular package, assuming free space over the insulator layer. Yan *et al.* provided a theoretical basis at millimeter-wave frequencies [54], whereas others provided simulation-based studies [27], [55], [56] or actual measurements using planar antennas [23], [57] and bond-wire antennas [8]. In the terahertz band analysis of [25], the package structure is described, but then neglected for simplicity. Finally, monopoles placed in a loosely defined
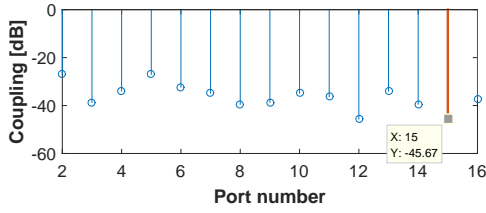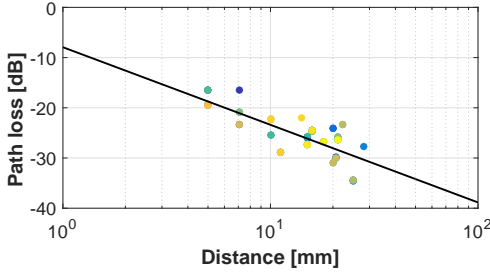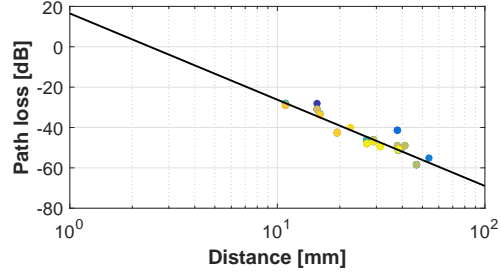
(a) Single standard chip on package substrate.
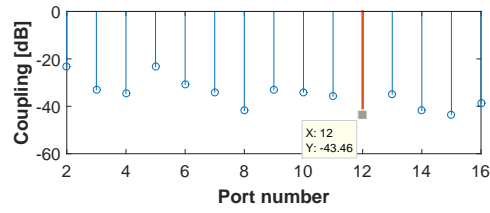
(b) Four small chips on silicon interposer.

Fig. 9. Mean of the S-parameter for each antenna pair assuming transmission from port 1 at 60 GHz. S_{min} is highlighted.

(a) Four small chips on silicon interposer.

(b) Four standard chips on MCM package.

Fig. 10. Path loss as a function of distance, including linear regression fitting, for the multi-chip cases at 60 GHz.

superstrate have been also studied in recent works [24], [47]. All these works, however, do not provide a faithful view of a chip package and cannot be re-used for the scenario at hand.

VI. Conclusion

The characterization of the wireless channel in scenarios compatible with standard chip packages is largely missing in the literature. To start bridging this gap, here we have performed a frequency-domain analysis of mm-wave propagation in the 3D stacking, silicon interposer, and multi-chip module schemes. We highlight the importance of package optimization to ensure the feasibility of the WNoC approach, as it is capable of reducing path losses by several tens of dBs. We also conclude that such optimization is dependent on the frequency of operation and the elements surrounding the chips. Finally, a path loss analysis confirms that propagation length within silicon is the main determinant of losses, and that finding the right package dimensions ensure the scalability of the approach.

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